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Method for manufacturing storage electrode of highly integrated semiconductor device

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Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2001008604	A	20010205	KR 9926523	A	19990702	200151 B

Priority Applications (No Type Date): KR 9926523 A 19990702

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
KR 2001008604	A	1	H01L-027/108	

Abstract (Basic): KR 2001008604 A

NOVELTY - A method for manufacturing a storage electrode of a highly integrated semiconductor device is to provide a storage electrode of a three-dimensional structure wherein the storage electrode has a broad sectional area and a uniform surface, by forming the storage electrode of a hemispherical grain(HSG) structure.

DETAILED DESCRIPTION - A **contact hole** of an interlayer dielectric(20) for isolation between devices is formed in a semiconductor substrate(10) having a semiconductor device. After a polysilicon layer highly doped with impurities is deposited in an active region to **contact** the **contact hole** and an undoped amorphous silicon layer is deposited, the stacked amorphous silicon layer and the polysilicon layer are patterned to guarantee a capacitor region of a stacked shape. A **sidewall spacer** (34) made of an undoped amorphous silicon layer is formed on a **sidewall** of the patterned amorphous silicon layer and polysilicon layer. After a silicon seed is formed on the amorphous silicon layer and a high vacuum annealing process is performed, the seed is uniformly grown as a hemispherical **convex** -concave shape to form a storage electrode.

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Title Terms: METHOD; MANUFACTURE; STORAGE; ELECTRODE; HIGH; INTEGRATE; SEMICONDUCTOR; DEVICE

Derwent Class: U13; U14

International Patent Class (Main): H01L-027/108

File Segment: EPI

Manual Codes (EPI/S-X): U13-C04B1A; U14-A03B4

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